supplied internal address when the selected mode control signal indicates a pipelined mode.

REMARKS

The Applicants' representative has carefully reviewed and considered the Office Action mailed on March 26, 2002, and the references cited therewith. Claim 60 has been canceled. Claim 63 is amended to correct a typographical error, and not for reasons related to patentability. No claims are added. As a result, claims 22-32, 59, 61, and 63-72 are now pending in this application. Claim 65 is allowed, and claim 64 is objected to as being based on a rejected claim (but is allowable if rewritten in independent form).

Summary of Embodiments of the Invention

As described in the Applicants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, embodiments of the invention disclosed relate to a memory device that selectably operates using both burst and pipelined modes of operation. In one embodiment, an asynchronously addressable storage device 100 (shown in FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Pg. 29, lines 5-25). The present invention can switch between burst access and ... pipelined modes of operation without ceasing ("on the fly"). (Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is first used to select data within the device 100. A counter 149 included in the circuitry 122 then increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses only external addresses 115 to access data within the device 100. (Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Pg. 8, lines 1-5). In addition to the embodiment described, the invention includes other embodiments of varying scope, including systems, methods, and storage devices, such as

memory circuits. (Pg. 33, line 23 - Pg. 40, line 19).

The Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20

U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). However, while it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. 171, 174 (C.C.P.A. 1979)). However, the level of skill is not that of the person who is an innovator but rather that of the person who follows the conventional wisdom in the art. *Standard Oil Co. v. American Cyanamid Co.*, 774 F.2d 448, 474, 227 U.S.P.Q. 293, 298 (Fed. Cir. 1985). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). The Examiner can only rely on references which are either in the same field as that of the invention, or if not in the same field, the references must be "reasonably pertinent to the particular problem with which the inventor was concerned." *M.P.E.P.* § 2141.01 (a) (citing *In re Oetiker*, 24 U.S.P.Q.2d (BNA) 1443 at 1445). The Examiner must also recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d (BNA) 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990).

If the proposed modification renders the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed

modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)). The Examiner must also avoid hindsight. *Id.* The Examiner cannot use the Appellant's structure as a "template" and simply select elements from the references to reconstruct the claimed invention. *In re Gorman,* 933 F.2d 982, 987, 18 U.S.P.Q.2d (BNA) 1885, 1888 (Fed. Cir. 1991).

The References

Manning (864) (U.S. Patent No. 5,610,864): discloses a memory device which may accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34).

The possibility of applying a pipelined architecture to Manning's invention is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50).

Manning (503) (U.S. Patent No. 5,729,503): describes a synchronous memory device having burst mode access and page mode access capabilties. (Col. 3, lines 3-4). In more complex versions of the device, fast page mode, EDO page mode, and static column mode may also be selected. (Col. 6, lines 52-56).

Discussion of the Rejections

1. The rejection under § 102:

Claims 22-32, 59-61, and 66-72 were rejected under 35 USC § 102(a) as being anticipated by Manning (864). First, the Applicants do not admit that Manning (864) is prior art

and reserve the right to swear behind this reference in the future. Second, the Applicants respectfully submit that a case of anticipation under 35 U.S.C. § 102(a) has not been made because Manning (864) fails to disclose each and every element of claims 22-32, 59, 61, and 63-72. Therefore, the Applicants respectfully traverse this rejection under 35 U.S.C. § 102(a).

1(a). Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

Manning (864) specifically fails to disclose "control logic for providing a ... mode control signal" and "a multiplexer ... for receiving ... the ... mode control signal ... therefrom and for switching the memory circuit between a burst mode and a pipelined mode", which is explicitly claimed by the Applicants in claims 22-32, and 59; or "control logic for providing [a] ... mode control signal" that is ultimately used to switch between, or indicate, burst and pipelined modes of operation, as claimed by the Applicants in claims 66-72.

Several assertions were made which attribute support to various concepts allegedly disclosed by Manning (864) in the Office Action mailed to the Applicants on 3/26/02 (Paper 24, pages 2-7). However, a careful reading of each citation reveals that the discussion of the asserted elements is either vague, nonexistent, or completely in error. These assertions have been made with respect to:

Claims 22, 59, and 66 - Manning (864) does not disclose a mode control signal, or circuitry for switching or selecting between a burst mode and a pipelined mode (Manning (864) never discusses switching or selecting between the modes, only operation in the burst mode, and the possibility of using a pipelined architecture). In fact, the Office has admitted this defect in Manning (864) in other Office Actions, such as the Office Action mailed to the Applicants on July 18, 2001 (Paper 19, page 7) for application serial no. 08/984,701, wherein the statement is made that "*Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation.*"

Claim 23 - Manning (864) does not disclose an external mode select signal for selecting the burst mode or the pipelined mode (the citation merely discusses switching between burst and standard EDO modes, or between interleaved and linear addressing modes).

Claims 25 and 70 - Manning (864) does not disclose using write enable and a separate *output enable* signal for determining the mode control signal (Manning only discusses using the write enable (/WE) and row address select (/RAS) signals for this purpose).

Claim 28 - Manning (864) does not disclose using a second external address subsequent to a first external address for operating in the pipelined mode (Manning never discloses how a pipelined *architecture* might operate).

Claims 29 and 72- Manning (864) does not disclose the pipelined mode as being an EDO mode (Manning never discloses how a pipelined *architecture* might operate).

Claims 30-31 - Manning (864) does not disclose any type of address strobe latency in conjunction with pipelined mode operations (Manning never discloses how a pipelined *architecture* might operate).

Claims 61 and 68 - Manning (864) does not disclose any type of control logic for providing an *internal* mode control signal (Manning only speaks to the use of *external* mode control signals).

1(b). Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Applicants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning (864) does not disclose these elements, how (specifically) does Manning (864) support *switching* or *selecting* between, or indicating burst and pipelined modes of operation, as claimed in claims 22, 59, and 66-72 (and in all claims that depend from them)?

Second, the Office has failed to establish a case of anticipation. While the assertion is made that Manning (864) discloses circuitry for "switching the memory circuit between a burst mode and a pipelined mode", and "a multiplexer", the Applicants' representative, after a careful study of Manning (864), was unable to locate any such discussion, nor any such circuitry which was configurable to select or switch between burst and pipelined modes of operation.

For example, the only citations offered by the Office to support the assertion that Manning (864) discloses "switching between a burst mode and a pipelined mode" with respect to claims 22, 59, and 66 are: col. 5, lines 41-50; col. 6, lines 14-34; and col 7, lines 43-54. Col. 5, lines 41-50 discusses the possibility of using a pipelined architecture as an *alternative* to burst operation, but not as enabling switching between pipeline or burst operations within the *same* memory, as disclosed and claimed by the Applicants. Col. 6, lines 14-34 merely describe burst and "standard" EDO operations (i.e., page mode - see col. 6, lines 18-19). Finally, col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning (864) never discusses the ability to *select* or *switch* between burst and pipelined modes of operation, or circuitry to effect such a selection, as claimed by the Applicants in independent claims 22, 59, and 66, and all of the claims which depend from them. As noted above, *this fact has been admitted by the Office.*

In short, what is discussed by Manning (864) is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection under § 102 is improper. Reconsideration and allowance of claims 22-32, 59, 61, and 66-72 is respectfully requested.

2. The rejection under § 103:

Claims 22-32, 59-61, 63, and 66-72 were rejected under 35 USC § 103(a) as being unpatentable over Manning (503) in view of Manning (864). First, the Applicants do not admit that Manning (864) or Manning (503) are prior art and reserve the right to swear behind these references in the future. Second, because the devices and methods taught in the references are not the same as that claimed by the Applicants, and can not be combined to operate as such, since there is no evidence in the record to support combining the references, and finally, since Manning (864) and Manning (503) teach away from any such combination, the Applicants respectfully traverse this rejection under § 103 by the Office.

Manning (503) teaches synchronous (not asynchronous) standard EDO, fast page mode EDO, and burst EDO modes of operation. As admitted by the Office, Manning (503) "does not specifically disclose a pipeline mode." Thus, it would be impossible for Manning (503) to

suggest or teach switching between a burst and a pipelined mode of operation. The Applicants can find nothing in the specification of Manning (503) to support asynchronously switching between burst and pipelined modes of operation. Instead, the device operates as a synchronous burst access memory device, as is clear from a reading of the Manning (503) title and disclosure. Since no mention is made in any of the references to asynchronously switching, selecting, or choosing between burst and pipelined modes of operation, combining Manning (864) and the Manning (503) references does not result in a device having asynchronously selectable burst and pipelined modes of operation. It is only hindsight gained from the Applicants' disclosure which enables providing both burst and pipelined modes of operation in a single asynchronous memory device, and switching therebetween at will.

Further, it is improper to combine Manning (864) and Manning (503). Manning (503) teaches a synchronous memory device. *See*, for example, the Title of Manning (503). Manning (864) is directed toward an asynchronous memory device. The M.P.E.P. requires that the asserted combination of the references must not render the prior art unsatisfactory for its intended purpose, or change the principle of operation of the reference being modified. *See* M.P.E.P. § 2143.01. One of ordinary skill in the art would not be led to combine the dissimilar operation of these two references because doing so would clearly change the fundamental principle of operation for each device disclosed, rendering one or the other unfit for its intended purpose. In addition, it is improper to combine references where the references teach away from their combination. See M.P.E.P. § 2145(X)(D)(2). In this case, each reference teaches away from the other: Manning (864) teaches asynchronous operation, while Manning (503) teaches synchronous operation.

Still further, the only reason given to combine the references so as to provide an asynchronous memory device which supports switching between a burst and pipelined mode of operation is because "it would increase the throughput by accessing data per every cycle thereby increasing system throughput". Since no reference is supplied to support this assertion, as required by the *In Re Sang Su Lee* court, it appears the Examiner is using personal knowledge, and the Examiner is thus respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2). Also, modifying a burst mode device to provide a pipelined mode of operation

would *decrease* the access speed, not increase the access speed, which is antithetical to progress in the art of memory chip design.

Finally, as was disclosed in the Application and noted in a several previous responses to various Office Actions in this matter, it is a specific unaddressed problem of asynchronous DRAMs to switch between burst and pipelined modes of operation, since it was not previously needed (see Background of The Invention, page 5, lines 16-22). Manning (503), describing a synchronous memory, most certainly is not directed toward the solution of this problem.

Since combining the references is improper, since any combination of the disclosed concepts would be inoperative, since the cited references fail to teach all aspects of the Applicants' invention as claimed, and since the references teach away from the combination asserted by the Office, the Applicants respectfully request reconsideration and withdrawal of the rejection of claims 22-32, 59, 61, 63, and 66-72 under 35 U.S.C. §103.

Summary

It is respectfully submitted that the art cited does not anticipate the claimed invention, nor does the cited art render the claimed invention obvious. It is respectfully submitted that claims 22-32, 59, 61, 63-65, and 66-72 should therefore be allowed. Reconsideration and withdrawal of the rejections of claims 22-32, 59, 61, 63-65, and 66-72 is respectfully requested. Should the Examiner be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also respectfully requested.

CONCLUSION

The Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney, Mark Muller, at (210) 308-5677, or the undersigned attorney, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 24 day of June, 2002.

Tina Kobat
Name

_____
Signature